submit that the claims as amended herein are deemed to clearly meet the requirements of 35 U.S.C. 112, second paragraph.

Applicants further note the rejection of Claims 1 - 3 and 26 - 28 under 35 U.S.C. 102(b) as being allegedly anticipated by Watanabe et al, U.S. Patent No. 3,890,564 as detailed in the Office Action; although no art has been applied to the remaining claims which are deemed to be at this time also directed to patentable subject matter.

However, applicants respectfully submit that all of the claims as presently on file are deemed to clearly and patentably distinguish over either the cited Watanabe U.S. Patent No. 3,890,564, or the secondary background reference Ahrenkiel et al. U.S. Patent No. 5,929,652, as traversed hereinbelow:

Concerning Watanabe, the configuration and function of the system described in this patent is different from what applicants are claiming as the new art. As shown in Figure 1 of this prior art patent and described therein, three coils systems; L1, L2, L3 and L4 comprise the prior art. The sample, or wafer, is placed between coils L1 and L2 and the operation of this system is intended to measure the conductivity or resistivity of the wafer. As described, the prior art in Watanabe is designed in such a way as to accomplish this objective. This is different from the coil or magnetic system described in the present core, where the design is to use one coil so as to generate an induced voltage in a circuit (loop) contained on a special mask. Thus, all of the applicants' claims patentably distinguish over Watanabe.

Pertaining to the background reference (Ahrenkiel) this is also clearly inapplicable to the invention, as follows:

The configuration and function of this patent is different from the configuration and function of the present case is that, in this prior art, the wafer is placed on top of the coil, and the

position of the sample relative to the coil is adjusted so as to provide electromagnetic coupling between the coil and the wafer. In the prior art patent, the coil is energized through a bridge circuit with the coil forming one arm of the 4-arm bridge circuit. This is different from the present invention, where the wafer is placed either in an air gap of a magnetic core and the magnetic core is directly supplied by a high frequency voltage source to produce a magnetic field, or the wafer could be placed in the middle of a continuos rectangular magnetic core.

In view of the foregoing comments and amendments, which are deemed to be fully responsive to the outstanding Office Action, applicants respectfully submit that the present application is clearly directed to allowable subject matter, and the early issuance of the Notice of Allowance is earnestly solicited.

However, in the event that the Examiner has any queries concerning the instantly submitted amendment, applicants' attorney respectfully requests that he be accorded the courtesy of possibly a telephone conference to discuss any matters in need of attention.

Finally, in compliance with the requirements, applicants also enclose a **"Version with Markings Showing Changes Made"** to facilitate the Examiner's review of the amendment to the claims.

Respectfully submitted,

Leopold Presser
Registration No. 19,827
Attorney for Applicants

Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343
LP:lac/lf

Serial No: 09/811,915 **Docket:** BUR920000082US1 (13647)

"VERSION WITH MARKINGS SHOWING CHANGES MADE"

IN THE CLAIMS:

Claims 1, 2, 4, 5, 10, 11, 26, 27, 30, 35 and 36 have been amended as follows::

1. (Amended) A method for electrically stressing through a specified voltage at least one semiconductor chip on a wafer for controlled contactless burn-in, voltage screen and reliability evaluation of product wafers, said method comprising:

[applying] providing a magnetic circuit for magnetically inducing said voltage for applying to said at least one chip for the probing thereof in the absence of physically contacting the chip surface; and

a mask being interposed on said wafer for magnetically inducing said voltage to said at least one chip [through the interposition of a] , said mask [onto which] having the voltage [is] induced thereto and thereafter conducted to electrical contacts on said wafer.

2. (Amended) A method as claimed in Claim 1, wherein said [applied] magnetically induced voltage [produces specified voltage bias conditions by inducing the voltage] is produced for a circuit utilizing a time varying magnetic field which is fixed with respect to said circuit.

4. (Amended) A method as claimed in Claim 1, wherein [said induced voltage is obtained at a top layer of] said mask which contains said circuit is positioned on said wafer; and

connections are made to said at least one chip by said mask for effectuating said burn-in without interference with the normal operation of said at least one semiconductor chip.

5. (Amended) A method as claimed in Claim 2, wherein said magnetic circuit comprises a loop defining an area on [a] said wafer, said mask being positioned on said wafer so as to enclose said area and having electrical contacts for an induced voltage through said time varying magnetic field within said enclosed area.

10. (Amended) A method as clamed in Claim 2, wherein said magnetic field is produced by a magnetic system which [circuit] comprises a circular magnetic core having an air gap for receiving said wafer with said at least one chip and said mask positioned thereon; and a voltage source connected to an electrical coil for energizing said magnetic core to produce said [specified] induced voltage [bias conditions].

11. (Amended) A method as claimed in Claim 10, wherein said [voltage is supplied to said electrical energizing coil from] said magnetic core is energized through a radio frequency voltage source.

26. (Amended) A system for electrically stressing through a specified voltage at least one semiconductor chip on a wafer for controlled contactless burn-in, voltage screen and reliability evaluation of product wafers, said system comprising:

[an arrangement] a circuit for applying said voltage to said at least one chip for the probing thereof in the absence of physically contacting the chip surface; and

a mask being arranged on said wafer through which said voltage is magnetically [inducing said voltage] induced and applied to said at least one chip through the interposition of [a] said mask onto which the voltage is induced and thereafter conducted to electrical contacts on said wafer.

27. (Amended) A system as claimed in Claim 26, wherein said [applied] induced voltage [produces specified voltage bias conditions by inducing the voltage] is produced for a circuit by utilizing a time varying magnetic field which is fixed with respect to said circuit.

30. (Amended) A system as claimed in Claim 27, wherein said circuit comprises a loop defining an area on a wafer, said mask being positioned on said wafer so as to enclose said area; wherein said loop includes and a loop having electrical contacts for an induced voltage through said time varying magnetic field being provided within said enclosed area.

35. (Amended) A system as clamed in Claim [27] 28, wherein said [circuit] magnetic field is produced by a magnetic system which comprises a circular magnetic core having an air gap for receiving said wafer with said at least one chip and said mask positioned thereon; and an electrical coil for energizing said magnetic core to produce said [specified] induced voltage [bias conditions].

36. (Amended) A system as claimed in Claim [35] 25, wherein said [voltage is supplied to said electrical energizing coil from] electrical core is energized through a radio frequency voltage source.